

What is Claimed is:

1. An integrated circuit for differential variable capacitors, comprising:
a p-substrate;
- 5 an n-well region, disposed at the top surface of said p-substrate;
at least three n-type ion implant regions, each disposed on the top surface of
said n-well region;
a metal wire, for connecting said at least three n-type ion implant regions;
a bias voltage control terminal, coupled to said n-type ion implant region;
- 10 a first gate; and
a second gate, being coupled to said first gate.
2. The integrated circuit for differential variable capacitors of claim 1,
wherein said first gate and second gate are disposed symmetrically on
opposite side of said voltage control terminal in respective.
- 15 3. The integrated circuit for differential variable capacitors of claim 1,
wherein said first gate is made of a polysilicon.
4. The integrated circuit for differential variable capacitors of claim 1,
wherein said second gate is made of a polysilicon.
5. The integrated circuit for differential variable capacitors of claim 1,
20 wherein said p-substrate further comprises a p-type ion implant region
arranged at the top surface thereof.
6. The integrated circuit for differential variable capacitors of claim 5,
wherein said p-type ion implant region is coupled to a grounding terminal.
- 25 7. An integrated circuit for differential variable capacitors, comprising:
an n-type substrate;
a p-type well region, disposed on the top surface of said n-type substrate;
at least three p-type ion implant regions, each disposed on the top surface of
said p-type well region;
a metal wire, for connecting said at least three p-type ion implant regions;
- 30 a bias voltage control terminal, coupled to said p-type ion implant regions;
a first gate; and

a second gate, being coupled to said first gate.

8. The integrated circuit for differential variable capacitors of claim 7, wherein said first and second gates are disposed symmetrically on both sides of said bias voltage control terminal.

5 9. The integrated circuit for differential variable capacitors of claim 7, wherein said first gate is made of a polysilicon.

10. The integrated circuit for differential variable capacitors of claim 7, wherein said second gate is made of a polysilicon.

10 11. The integrated circuit for differential variable capacitors of claim 7, wherein said n-type substrate further comprises an n-type ion implant region arranged at the top surface thereof.

12. The integrated circuit for differential variable capacitors of claim 11, wherein said n-type ion implant region is coupled to a grounding terminal.